SUBSTANCE OF INTERVIEW IN RESPONSE TO
INTERVIEW SUMMARY DATED DECEMBER 22, 2005
(PAPER NO. 20051223)

In the claims:

Amended claims 23, 39 and 55, with the agreed upon new language identified by underlined text, are reproduced below:

23. A method for suspending operation of a pipelined data processor to reduce power consumption, comprising:

enabling a first clock signal in response to an occurrence of a first combination of respective states of one or more clock control signals;

advancing a sequence of instructions to a first portion of a pipeline subcircuit;

executing said advanced sequence of instructions with a second portion of said pipeline subcircuit subsequent to said first pipeline subcircuit portion in response to said enabled first clock signal; and

detecting an occurrence of a second combination of said respective states of said one or more clock control signals and in response thereto

interrupting said advancing of said sequence of instructions to said first pipeline subcircuit portion, followed by

completing executing of said advanced sequence of instructions which had been advanced to said first pipeline subcircuit portion, wherein said advanced sequence of instructions being executed had been advanced to said first pipeline subcircuit portion prior to said interrupting ~~of said advancing of said sequence of instructions to said first pipeline subcircuit portion~~, followed by

executing with said second pipeline subcircuit portion a plurality of microcode substantially unrelated to said advanced sequence of instructions in response to said enabled first clock signal, and followed further by

disabling said first clock signal.

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39. A method for suspending operation of a pipelined data processor to reduce power consumption, comprising:

enabling a first clock signal in response to an occurrence of a first combination of respective states of one or more clock control signals;

advancing a sequence of instructions to a first portion of a pipeline subcircuit;

executing said advanced sequence of instructions with a second portion of said pipeline subcircuit subsequent to said first pipeline subcircuit portion in response to said enabled first clock signal; and

detecting an occurrence of a second combination of said respective states of said one or more clock control signals and in response thereto

interrupting said advancing of said sequence of instructions to said first pipeline subcircuit portion, followed by

completing executing of said advanced sequence of instructions which had been advanced to said first pipeline subcircuit portion, wherein said advanced sequence of instructions being executed had been advanced to said first pipeline subcircuit portion prior to said interrupting ~~of said advancing of said sequence of instructions to said first pipeline subcircuit portion~~, and

generating a plurality of address data, followed by

executing with said second pipeline subcircuit portion a plurality of microcode corresponding to said plurality of address data and substantially unrelated to said advanced sequence of instructions in response to said enabled first clock signal, and followed further by

disabling said first clock signal.

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55. A method for suspending operation of a pipelined data processor to reduce power consumption, comprising:

enabling a first clock signal in response to an occurrence of a first combination of respective states of one or more clock control signals;

advancing a sequence of instructions to a first portion of a pipeline subcircuit;

executing said advanced sequence of instructions with a second portion of said pipeline subcircuit subsequent to said first pipeline subcircuit portion in response to said enabled first clock signal; and

detecting an occurrence of a second combination of said respective states of said one or more clock control signals and in response thereto

interrupting said advancing of said sequence of instructions to said first pipeline subcircuit portion, followed by

completing executing of said advanced sequence of instructions which had been advanced to said first pipeline subcircuit portion, wherein said advanced sequence of instructions being executed had been advanced to said first pipeline subcircuit portion prior to said interrupting ~~of said advancing of said sequence of instructions to said first pipeline subcircuit portion~~,

generating a plurality of address data, and

addressing said first pipeline subcircuit portion with said plurality of address data and in response thereto generating a plurality of microcode substantially unrelated to said advanced sequence of instructions, followed by

executing said plurality of microcode with said second pipeline subcircuit portion in response to said enabled first clock signal, and followed further by

disabling said first clock signal.

10/784,834 PATENT

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Respectfully submitted,

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